



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,391	10/22/2001	Jurgen Nolles	1999P1681P	9819

7590 02/17/2004

LERNER AND GREENBERG, P.A.
PATENT ATTORNEYS AND ATTORNEYS AT LAW
Post Office Box 2480
Hollywood, FL 33022-2480

EXAMINER

KERVEROS, JAMES C

ART UNIT	PAPER NUMBER
2133	7

DATE MAILED: 02/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

P29

Office Action Summary

Application No.	10/007,391	Applicant(s)	NOLLES ET AL.
Examiner	James C Kerveros	Art Unit	2133

-- The MAILING DATE of this communication appears in the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 22 October 2001.
2a) This action is FINAL. 2b) This action is non-final.
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-14 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) Claim(s) _____ is/are allowed.
6) Claim(s) 1-14 is/are rejected.
7) Claim(s) _____ is/are objected to.
8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
10) The drawing(s) filed on 22 October 2001 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 44

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-6, 8-11, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. (US 6311300).

Regarding independent Claims 1, 13 and 14, Omura substantially discloses a semiconductor testing apparatus for testing a semiconductor device including a built in self test circuit, comprising:

A logic circuit (logic IC unit 3) having a structure to be tested, as shown in FIGS. 1, 3 and 4 –7 and structural testing device (31), which is serial pattern generator, for testing the structure of the logic circuit (3), FIG. 6.

A functional circuit BIST (4), Built In Self Test circuit, connected to the structural testing device (31) through an indirect interface (P5, P6) corresponding to signals (S1, S0) with a scan in signal (SI) and a scan out signal (SO), where the functional circuit BIST (4) drives the logic circuit (3) through a direct interface, which couples the logic circuit (3) and the BIST (4) both located in (IC21).

The functional circuit BIST (4) receives the test commands from the external device (IC tester 30) through a standard interface (P2, P3), where the functional circuit BIST (4) forwards the test commands to the indirect interface (P5 and P6) using computer (11) for indirectly driving the logic circuit (3), FIG. 6.

Omura does not connect the functional circuit and the structural testing device through an indirect interface. However, he discloses a functional circuit BIST (4) and a structural testing device such as serial pattern generator (31) where the pattern generator (31) communicates with (logic IC unit 3) under test. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to rearrange the serial signals (S1, S0) from the pattern generator (31) in the IC device of Omura, by routing the signal wiring through functional circuit BIST (4), for the purpose of achieving indirect communication with the IC logic circuit under test, so as to save functional space on the IC, by integrating the serial signals with the BIST circuit.

Regarding Claim 2, Omura discloses a structural testing device, such as serial pattern generator (31), including a scan path (S1, S0) and test points (P5, P6), where part of logic IC (3) of ICs (21) is tested by tester (30) in accordance with the scan path method, and where a serial pattern generator (31) is newly provided in IC tester 30 (column 6, lines 5-10).

Regarding Claims 3, 4 and 6, Omura discloses a functional circuit BIST (4), which generates a test pattern in accordance with the input signals CLK and CMD from pattern generator 13, and applies the test pattern to memory IC unit 2 and logic IC unit

3, and then tests and analyzes the units 2 and 3, see FIG. 6 and 8 and also (column 4, lines 27-36).

Regarding Claim 5, Omura discloses a structural testing device, such as serial pattern generator (31) for generating a test pattern in the form of pseudo-random vectors.

Regarding Claims 9-11, Omura discloses a logic circuit under including multiple logic modules, shown in FIG. 7, wherein the functional circuit BIST (4) selects and tests a logic module.

Regarding Claim 8, Omura discloses a functional circuit BIST (4) including software for communicating with computer 11, which stores the serial/parallel data applied from BIST circuit 4, through the converter 14 and outputs parallel date to the computer.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. (US 6311300) in view of Barch et al. (US 5923836).

Regarding Claim 7, Omura does not perform functional test based upon a simulation result for the structural test device and the logic circuit. However, Barch (US 5923836), in an analogous art, discloses a computer simulation process of an IC design, by loading a simulated scan chain with the state data of the simulation test vectors. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the computer simulation process, as taught by Barch, in the functional circuit BIST of Omura, for the purpose of increasing the fault

coverage, by updating the test pattern through simulation so as to detect every potential fault for the logic circuit under test.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. (US 6311300) in view of Kirihata et al. (US 5764655).

Regarding Claim 12, Omura does not disclose a contactless interface. However, Kirihata (US 5764655), in an analogous art, discloses field testing of an integrated circuit chip by providing both an on chip RF receiver for communicating a retest command and an on chip RF transmitter for communicating the test results, RF Transceiver (26), which transmits and receives test data from SPBIST (22) via RF contactless method, FIG. 4. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate an RF Transceiver, as taught by Kirihata, in the integrated circuit of Omura, for the purpose of transmitting and receiving remotely test data and test commands to and from an external device, since the remote IC testing method eliminates the need for testers in the manufacturing environment, such that there are no bottle-necks in product flow in a production line.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

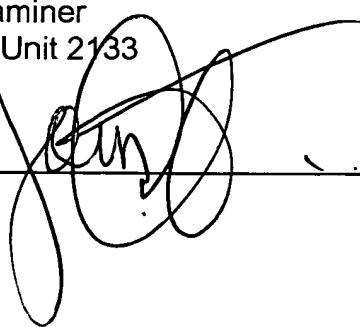
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 2/13/04
Non-Final Rejection

James C Kerveros
Examiner
Art Unit 2133

By: 

*louis J. Lamarre
for*

Albert DeCady
Primary Examiner